TECHNIQUES FOR IMPROVING THE STABILITY AND AMPLIFIER PERFORMANCE OF X-BAND GaAs POWER FETs

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ABSTRACT

Via hole source connections together with on-carrier matching significantly improve X-band power FET performance. Via hole connections eliminate spurious oscillations by reducing common-lead source inductance. On-carrier matching metworks improve the power and gain of X-band FET amplifiers by partially matching the very low input and output impedance of large periphery devices with impedance transformation networks located as close to the transistor as possible.

Introduction

In the design of GaAs FETs it is advantageous to reduce the common-lead source inductance in order to improve device stability and thus eliminate spurious oscillations. Previously published results[1] have experimentally verified that the via (plated through) hole source connection technique is effective in reducing parasitic source inductance and improving small signal gain for GaAs FETs at 4 GHz. Recent results obtained on two different power FET designs, one having a gate periphery of 3 mm and the other 4.8 mm show that via hole source connections significantly improve the stability of X-band power FETs when compared with devices employing conventional wire bonds to ground the sources. In addition, via hole devices tend to exhibit higher small signal gain and lower feedback, while simplifying mechanical assembly by reducing the number of wire bonds.

Due to the low input and output impedances of larger gate periphery power FETs it is critical to minimize the losses between the device and the impedance matching networks to obtain optimum performance. However, since commercially available power FETs are supplied either on carriers or in packages which are electrically long at X-band frequencies, external matching networks cannot be located near the plane of the device. A significant improvement in X-band performance has been obtained by locating matching networks, which partially match the FET chip to an intermediate impedance level, directly on the device carrier.

Stability Improvement With Via Hole Source Connections

Via hole connections consist of tiny holes etched through the GaAs wafer which are filled with gold in order to connect the device source pads directly to ground without the use of wire bonds. Although there are a number of benefits derived from the use of via holes, the most important is improved stability. Figures 1 and 2 show the I-V characteristics of two 3 mm power FET devices with wire bond and via hole source connections respectively. The bumps and jumps evident in the characteristics of the wire bonded device are due to spurious oscillations occurring in the 12 to 15 GHz frequency range. The output power level of these oscillations varies greatly with changes in dc bias and typically ranges from -20 dBm to 0 dBm. Although this is a relatively low level, it is conceivable that only a small portion of the oscillation occurring within the device is coupled out. Although the severity of these oscillations, as well as their impact on the dc characteristics, varies with the length and orientation of the source wire bonds, it has not been possible to find a repeatable bonding wire

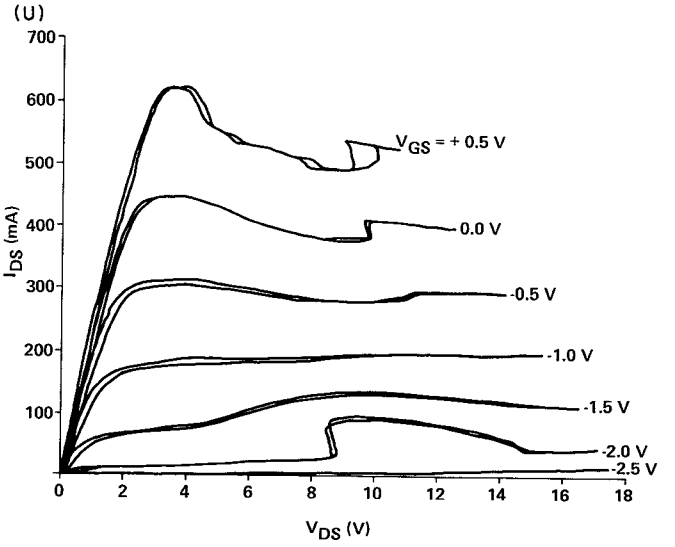

Figure 1: Typical I-V Characteristics Of Wire-Bonded GaAs Power FET

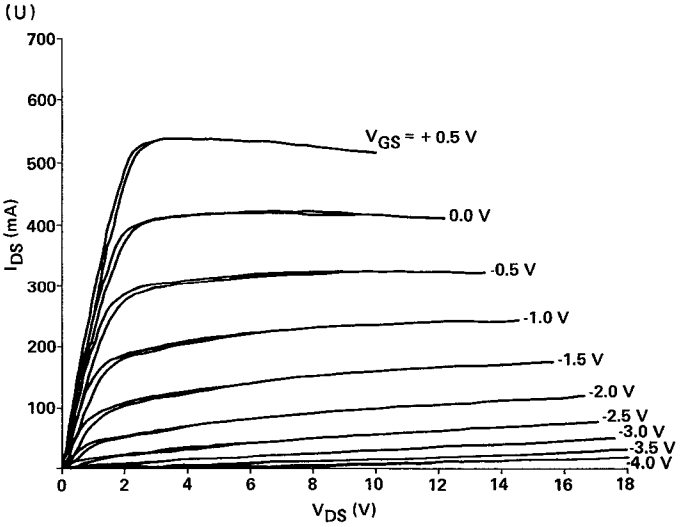

Figure 2: Typical I-V Characteristics Of Via Hole GaAs Power FET

arrangement which would eliminate the oscillations. Via hole connections on the other hand, have been extremely effective in suppressing the oscillations. Note the clean, smoothly varying I-V characteristics of Figure 2. Devices from a split wafer, one half of which was processed with via holes and one half without, have been tested and compared to be sure that the results discussed above could not be attributed to wafer differences rather than connection method differences. This test confirmed the effectiveness of via holes in preventing these spurious oscillations.

While via holes, or at least some very low inductance source connection technique other than wire bonds, may be necessary to insure stability under all possible dc bias conditions, they are by no means sufficient. It is still possible to encounter oscillation problems if the gate and drain connections are not handled properly. Figure 3 shows the mask layout of a 4.8 mm gate periphery device under investigation for X-band performance. Note that the individual cell gate and drain bonding pads are not connected together. Initial testing of devices made with this mask and using via hole source connections revealed the same sort of poor quality I-V characteristics of Figure 1. In this case the oscillation frequency was somewhat lower, 7 to 8 GHz. It was subsequently discovered that if the four gate bonding pads were tied together with a ribbon, the oscillations did not occur. This gate interconnection has subsequently been incorporated into the mask design.

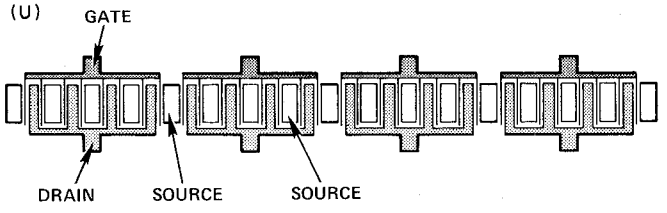

Figure 3: 4.8 mm Gate Periphery Mask For X-Band GaAs Power FET With Via Hole Source Connections

Amplifier Performance Using On-Carrier Matching

GaAs FETs from several wafers were mounted on gold-plated copper carriers for RF evaluation. The carriers were approximately 0.20 in. in length and contained 0.025 in. thick alumina substrates, with 50 ohm microstrip input and output lines. It was felt that small signal S-parameters are an adequate first order representation of the device characteristics under large signal conditions. Several FETs were therefore characterized in terms of their small signal S-parameters. The S_{11} and S_{22} for four different devices is given in Figure 4 referenced to the edges of the carrier. Typical values of S_{21} and S_{12} at 10 GHz were -10 dB at -59° and -34 dB at -34° respectively. The magnitude of S_{21} between 8 and 12 GHz is shown in Figure 5. The carrier mounted devices were then placed in a microstrip amplifier circuit and tuned for highest output power over a 5 percent band centered at 10 GHz. Typical performance achieved was 0.5 W with 3 dB gain. This observed output power was considerably poorer than expected based upon device dc characteristics.

It was concluded that one could improve the achievable amplifier bandwidth and minimize the loss introduced between the FET chip and the amplifier matching

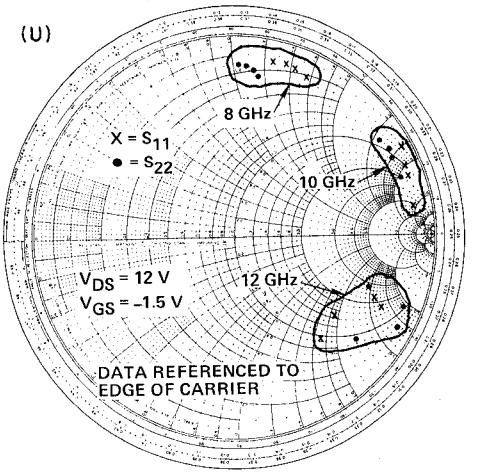

Figure 4: S-Parameter Data For Four 4.8 mm Via Hole Connected FETs

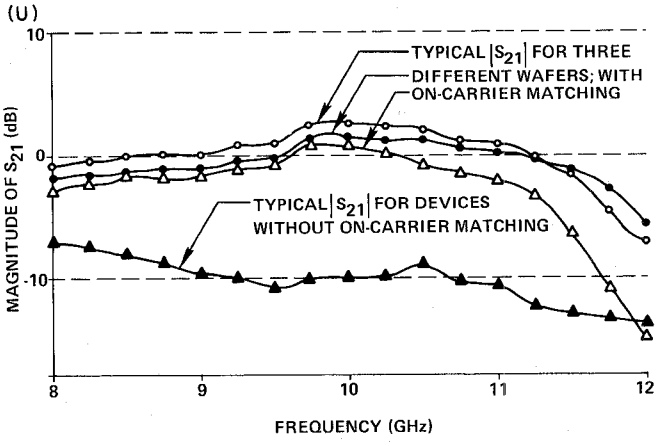

Figure 5: $|S_{21}|$ Versus Frequency For Devices With and Without On-Carrier Matching Networks

network by incorporating impedance transformation networks as close to the FET chip as possible. Therefore input and output matching networks were designed using the measured device S-parameters to partially match the device to an intermediate impedance of 20 ohms. These matching circuits were realized on the alumina substrates located on the device carrier.

The S-parameters of several FETs with identical on-carrier matching networks were measured. The magnitude of S_{21} for these devices was measured to be up to 10 dB higher between 8 and 12 GHz. In addition, the improvement in $|S_{21}|$ was found to be quite uniform for devices taken from different wafers, as shown in Figure 5. Two devices with on-carrier matching networks identical to those used above were also measured between 4 and 8 GHz and similar values of $|S_{21}|$ were observed.

Several partially matched, carrier mounted devices were placed in an amplifier circuit to determine the effect of on-carrier matching on amplifier performance. The amplifier was first optimized for

small signal gain over a 10 percent bandwidth. The resulting data at 10 GHz is shown in Figure 6 for two representative device samples and indicates an output power of +23 dBm with an associated gain of 12 dB (Device A) and +23 dBm of output power with 8 dB of gain (Device B). The output matching networks were then adjusted for highest output power. Under these conditions Device A provided +30 dBm of output power with 6 dB of gain at 10 GHz, while Device B provided +28 dBm with an associated gain of 6 dB. In all cases only the amplifier matching networks were tuned while the on-carrier matching networks were not adjusted. Under both tuning conditions Device A was operated with a drain bias of 12 V, gate bias of -2.0 V and drain current of 400 mA. Similarly Device B was biased at V_{DS} = 8 V, V_{GS} = -1.0 V and I_{DS} = 295 mA.

Conclusions

The use of via hole source connections on 3 and 4.8 mm gate periphery power FETs has yielded stable devices which are free of the high frequency oscillations commonly observed on conventionally wire-bonded transistors. Careful monitoring of device I-V characteristics with the device mounted in a 50 ohm RF test fixture is a convenient and simple means of investigating their stability. In order to insure spurious-free RF operation of a power FET, its I-V curves must be clean and well behaved for all combinations of drain and gate voltages. In addition to stability, via hole source connections result in better small signal gain and lower feedback while easing the assembly task by eliminating the need for source wire bonds.

The utilization of on-carrier matching networks which match the device input and output impedances to an intermediate level of 20 ohms has proven to be effective in improving the power gain performance of power FET amplifiers at X-band. Furthermore, the $|S_{21}|$ of FETs with these matching networks has been shown to be approximately 10 dB higher than that of the device itself over greater than 40 percent bandwidth. This implies that the on-carrier partial matching technique may result in improved performance for amplifiers designed for broad bandwidths.

The results presented for devices with on-carrier matching networks also indicate that it is desirable for device manufacturers to incorporate simple microstrip matching networks within the confines of the device package. This will substantially reduce the degradation in X-band performance which must presently be accepted, if hermeticity and handling considerations require the use of packaged FETs.

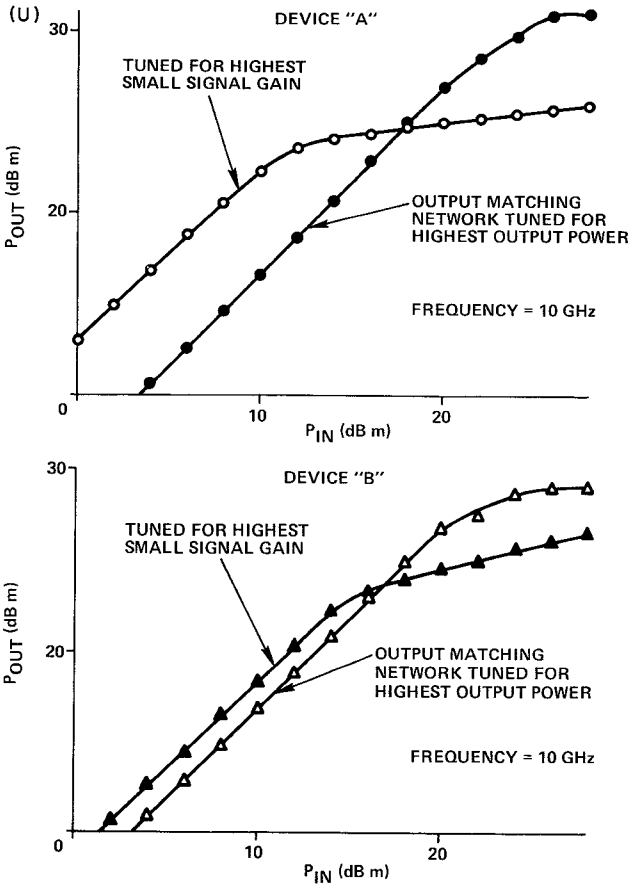

Figure 6: Power Amplifier Performance

Acknowledgements

The authors wish to acknowledge the contributions of R. Thomas who perfected the via hole processing technique, R. Ellis for contributions to FET processing, L. Reynolds for assistance in RF testing and M. Benedek for many enlightening technical discussions. Thanks are due also to D. M. Raymond for the mechanical design and assembly of the amplifier circuits and S. Fumia for his efforts in the area of artwork generation.

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